EE 230
Lecture 32

Nonlinear Circuits and Nonlinear Devices

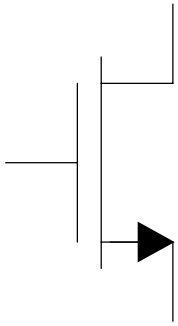
- Diode
- BJT
- MOSFET

Thanks for your input !

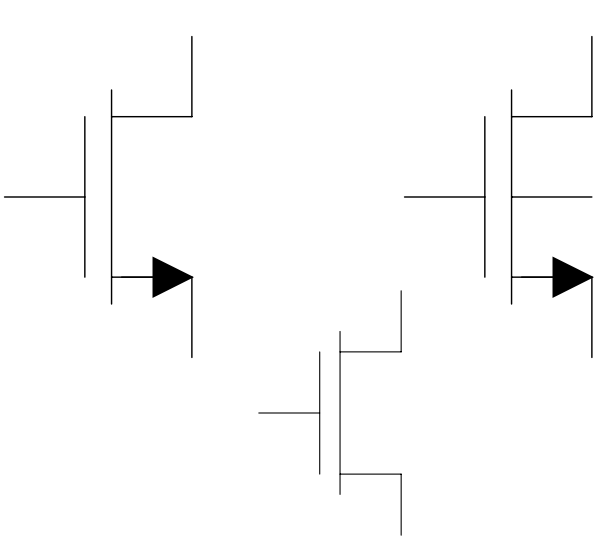
	Mean	Var	Min	Max
How many hours do you spend per week working with lecture material (including time spent in the lecture and HW)	8.6	3.3	4.5	20.0
Of those in the first question, how many are spent in group study?	2.5	2.1	0.0	7.0
How many hours per week do you spend working in the lab on laboratory experiments	5.4	3.7	2.5	20.0
How many additonal hours per week do you spend on laboratory requirements?	3.1	2.3	0.0	11.0
What percent of the lectures do you attend?	93.0	15.5	10.0	100.0
How many hours do you spend reading materials from text or notes not associated with solving homework assignments	1.4	2.0	0.0	10.0
What was your grade average, before the retake, on the first two exams	58.0	12.3	20.0	82.0
Total Hours	17.1	6.2	8.0	35.0

Review from Last Time:

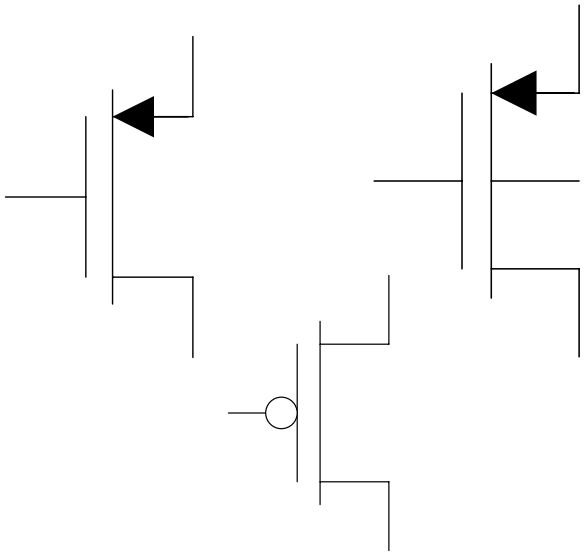
MOS Transistors



MOSFET



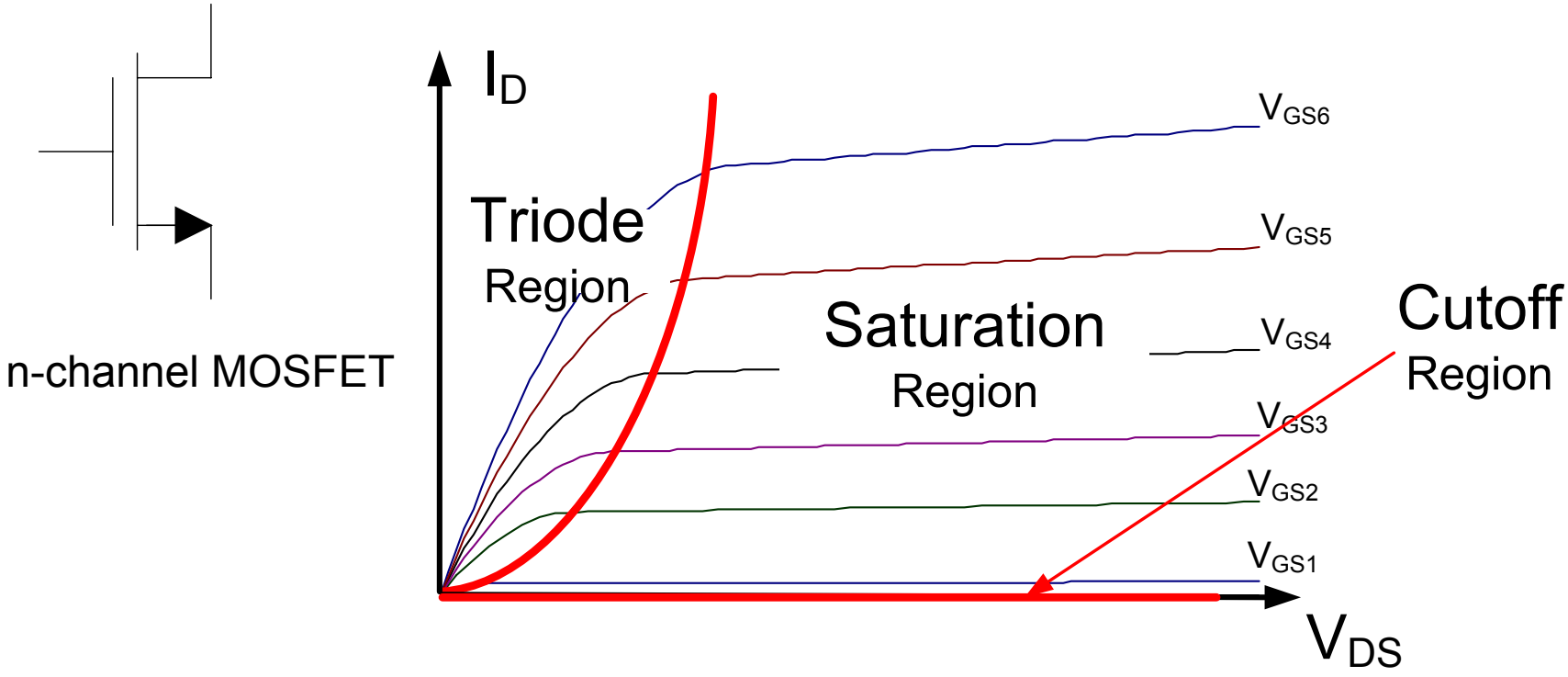
n-channel



p-channel

Review from Last Time:

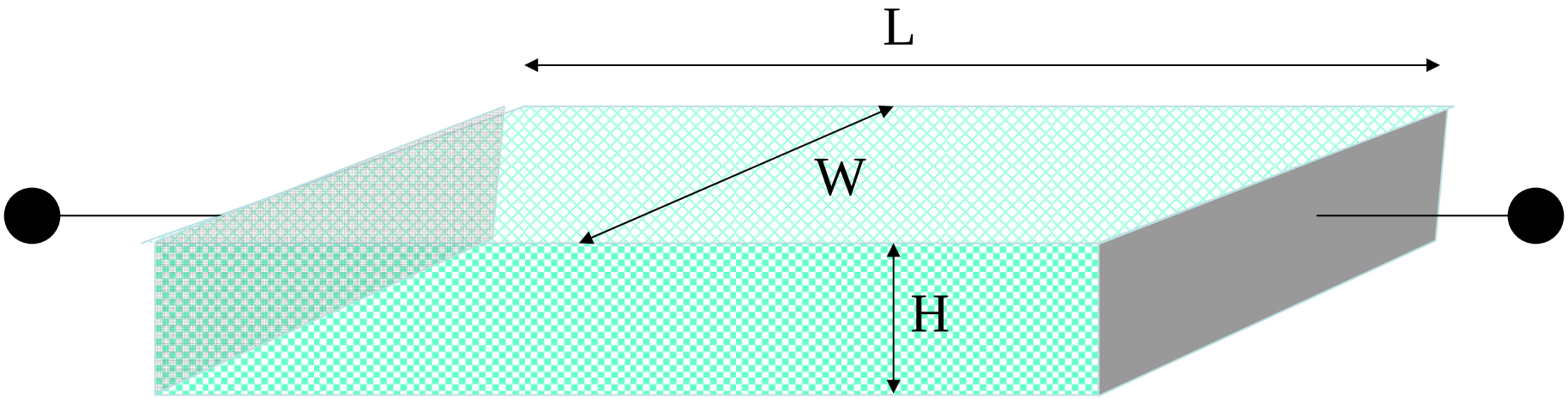
MOS Transistors



In most analog applications, the MOSFET is operated in the saturation region

In most digital applications, the MOSFET is operated in either the cutoff or triode regions and changes between these two regions as the boolean variables change from a “0” to a “1”

n-type resistor

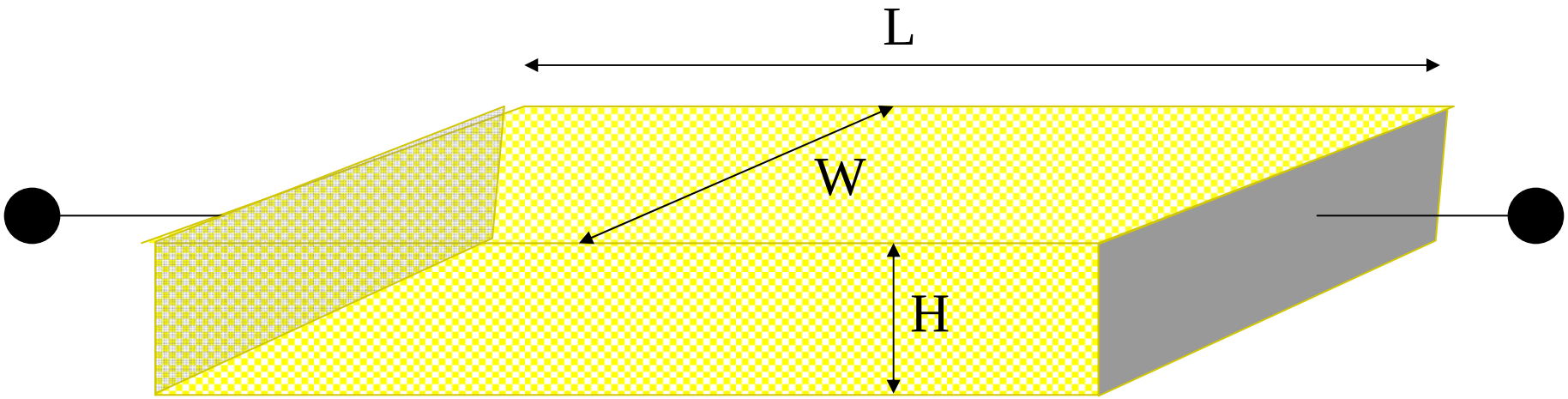


$$R = \rho \frac{L}{WH}$$

p-type semiconductor

If H is small compared to L and W, termed a thin-film resistor

p-type resistor

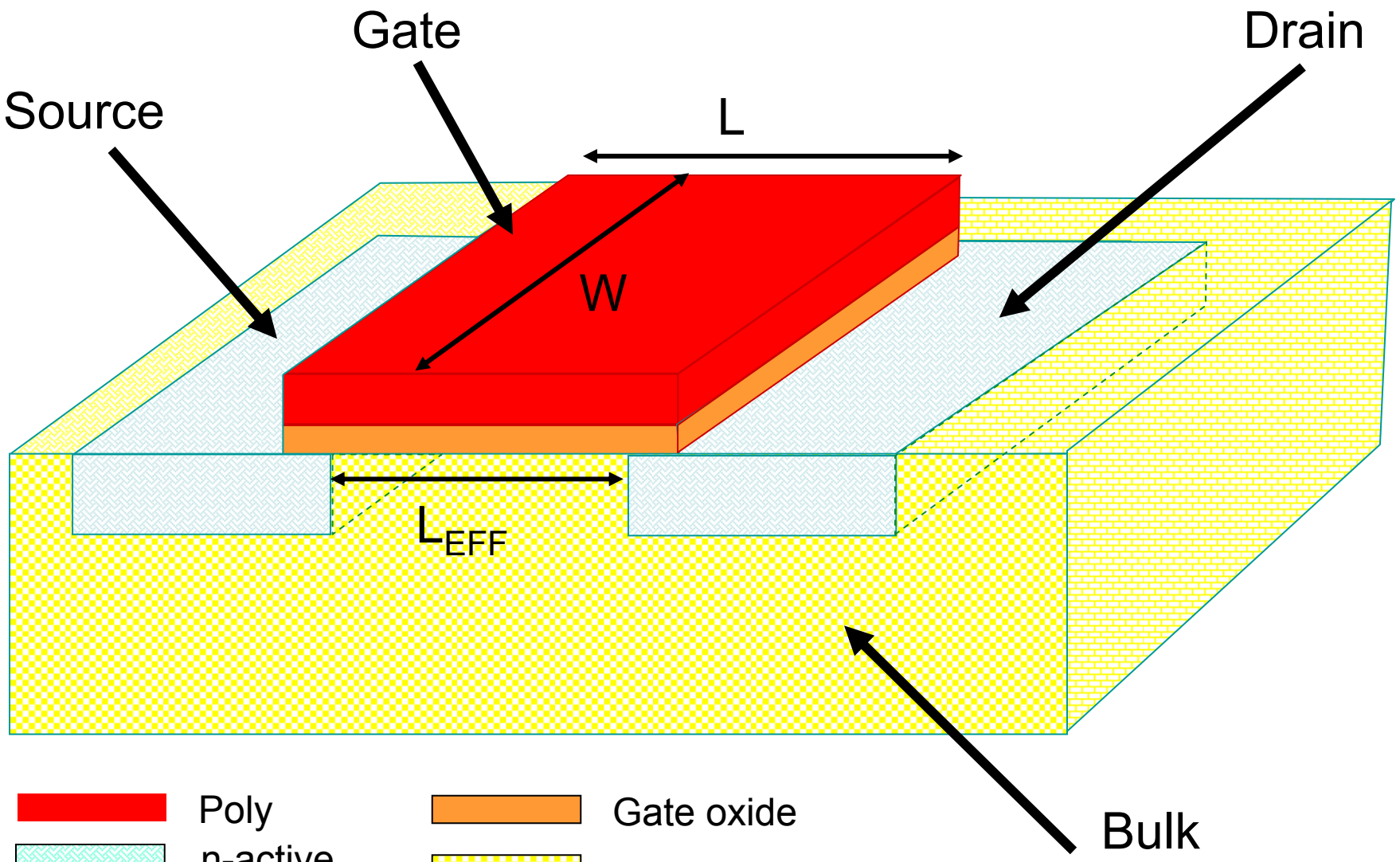


$$R = \rho \frac{L}{WH}$$

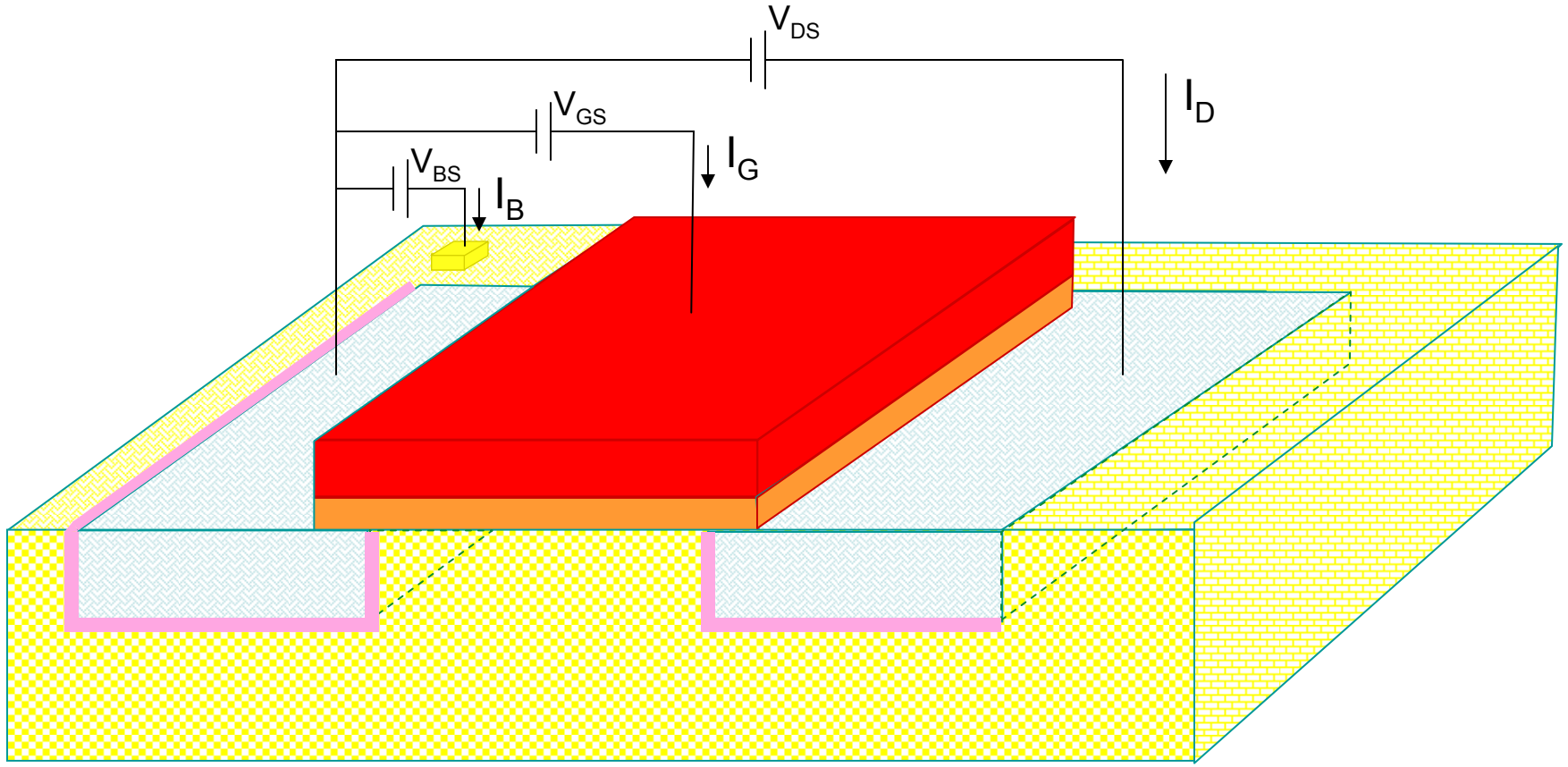
p-type semiconductor

If H is small compared to L and W, termed a thin-film resistor

n-Channel MOSFET



n-Channel MOSFET Operation and Model

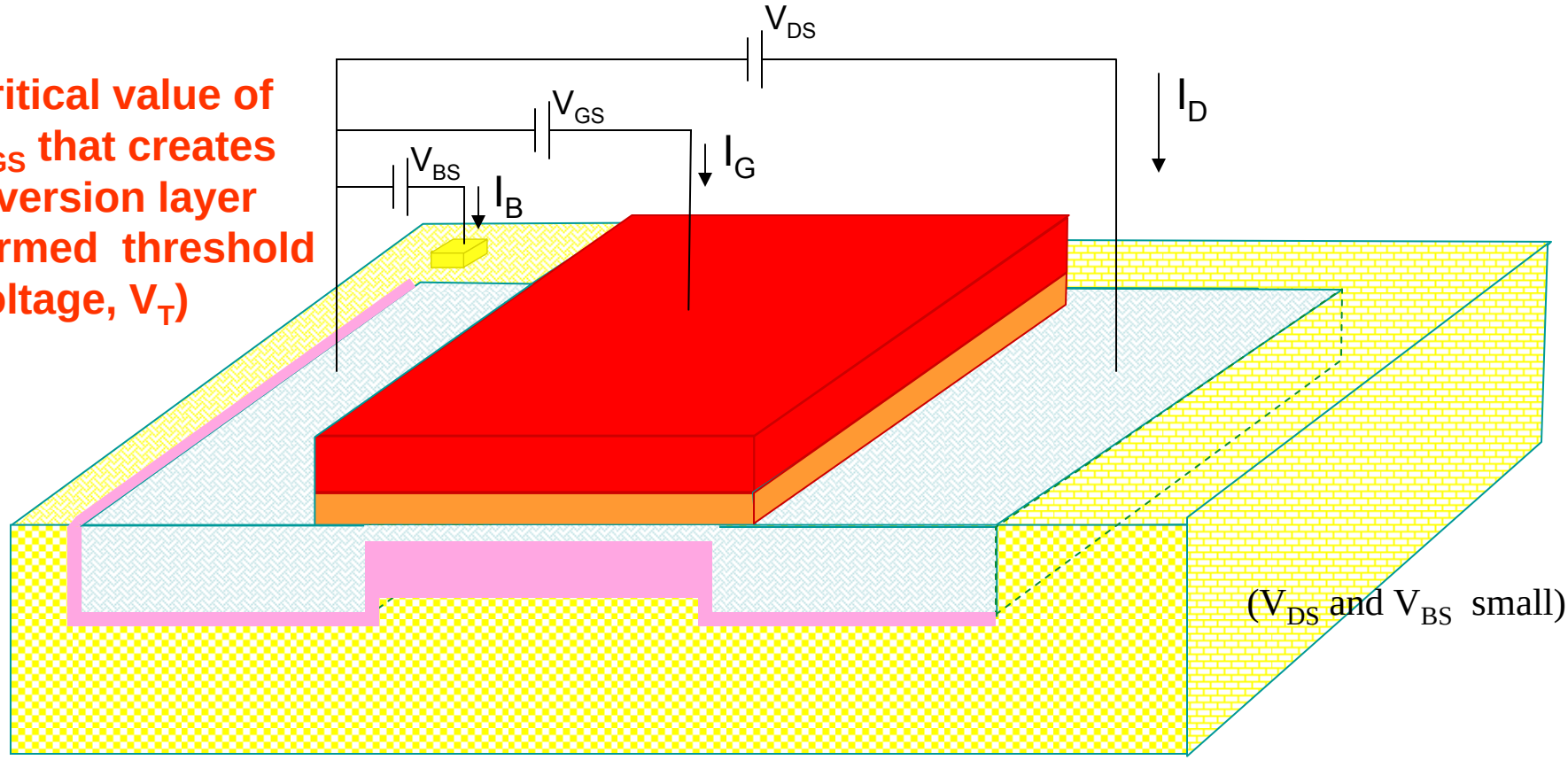


“Cutoff” region of operation

$I_D=0$
$I_G=0$
$I_B=0$

n-Channel MOSFET Operation and Model

Critical value of V_{GS} that creates inversion layer termed threshold voltage, V_T)



"Triode" region of operation

Inversion layer forms in channel

Inversion layer will support current flow from D to S

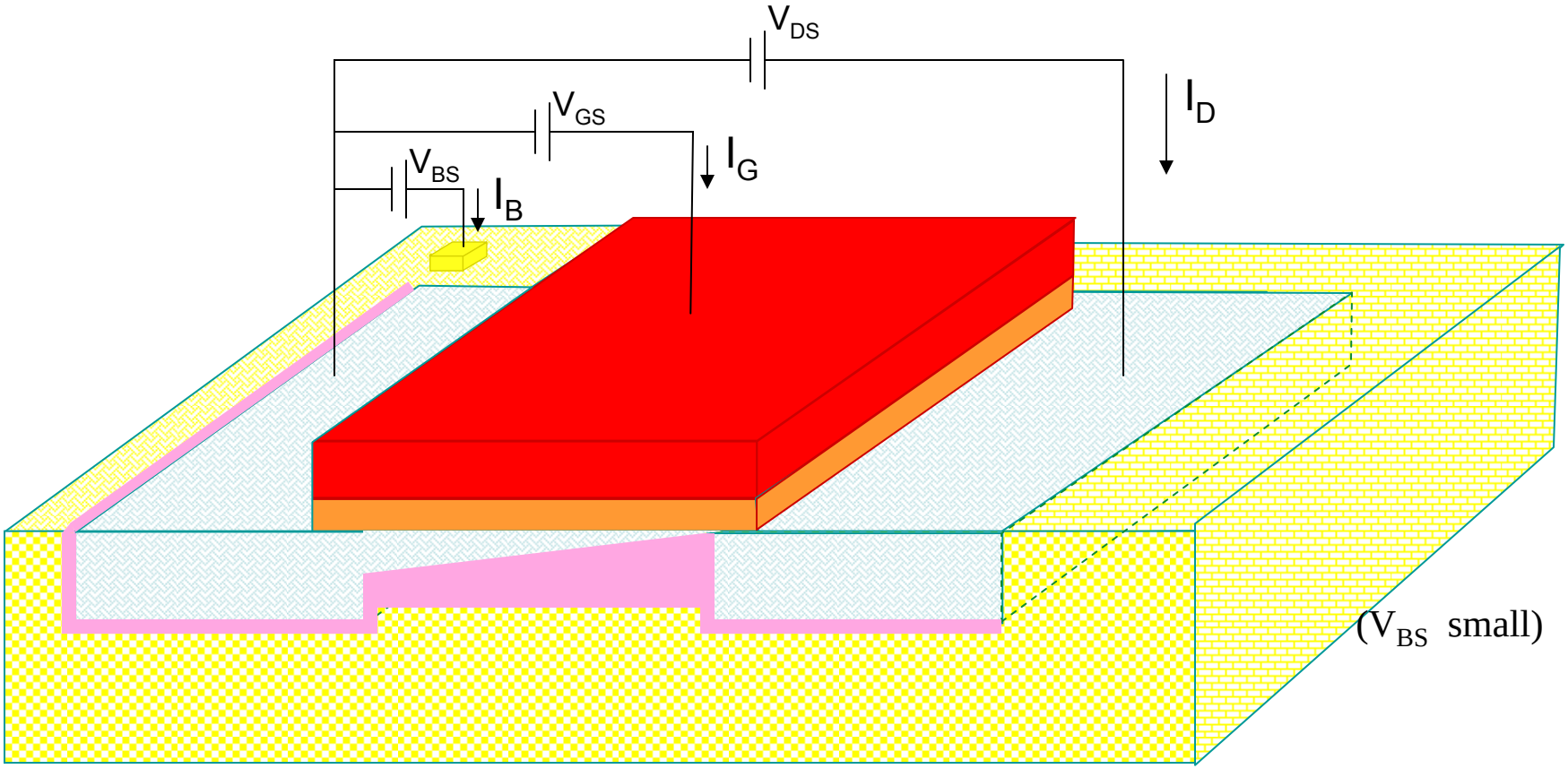
Channel behaves as thin-film resistor

$I_D R_{CH} = V_{DS}$

$I_G = 0$

$I_B = 0$

n-Channel MOSFET Operation and Model



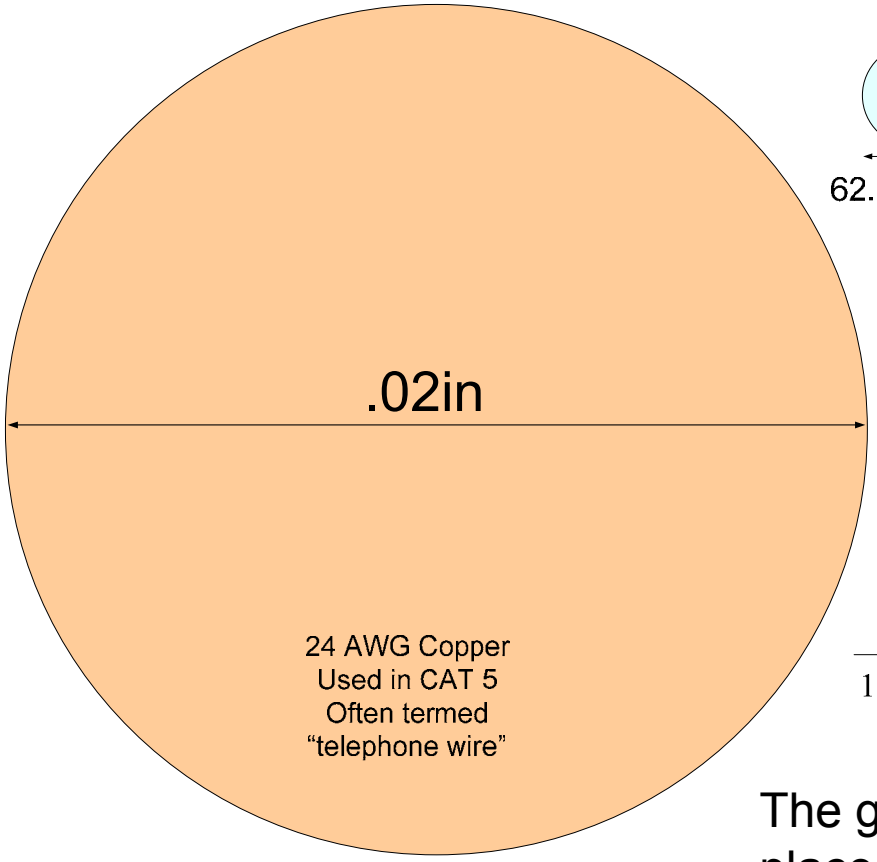
"Saturation" region of operation

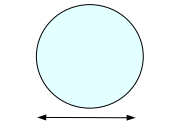
I_D=?
I_G=0
I_B=0

Inversion layer disappears near drain

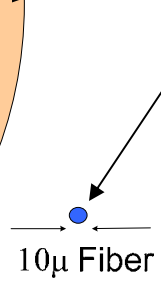
Saturation first occurs when $V_{DS}=V_{GS}-V_T$

Transistor Size Comparison with 24AWG Copper Cable (Drawn to scale)



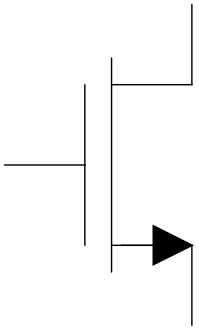


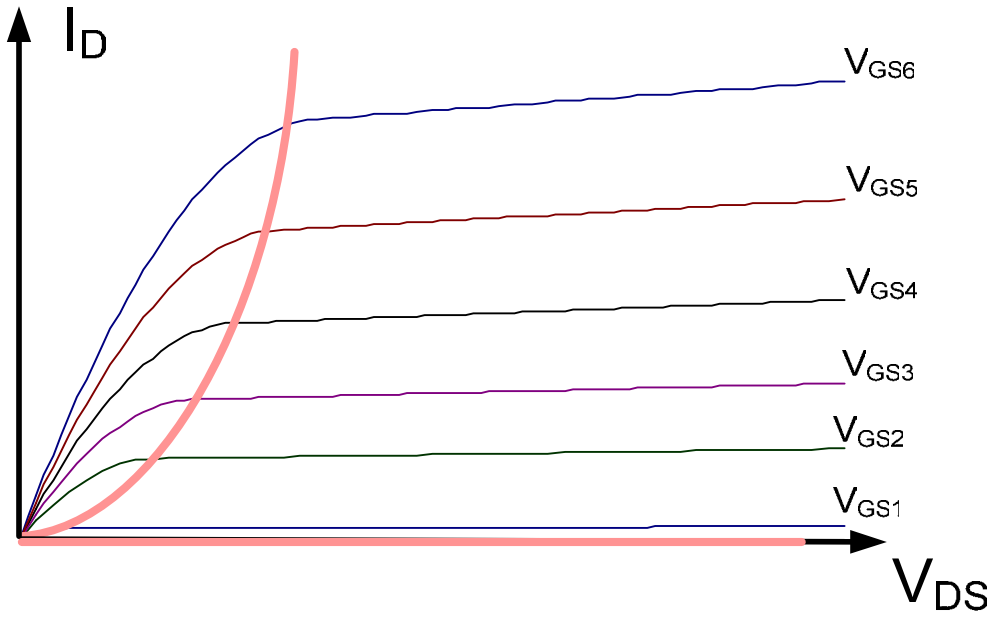
State of Art transistor dimensions about 200 times smaller (lateral) than 10µ fiber



The gates of about 40000 transistors can be placed on the cross-section of this fiber (maybe only 4000 transistors)

MOS Transistors





Standard square-law model

$I_G = 0$

$$I_D = \begin{cases} 0 & V_{GS} < V_T \\ \left(\frac{\mu C_{OX} W}{L}\right)\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T \quad V_{DS} \leq V_{GS} - V_T \\ \left(\frac{\mu C_{OX} W}{2L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS}) & V_{GS} \geq V_T \quad V_{DS} > V_{GS} - V_T \end{cases}$$

Cutoff

Triode

Saturation

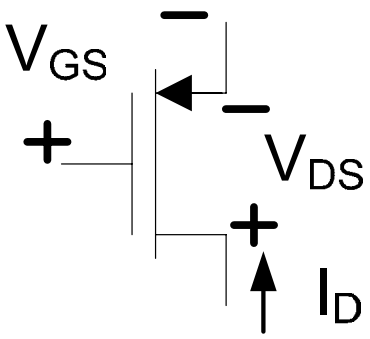
$\mu C_{OX} \approx 10^{-4} \, A/V^2$

$\lambda \approx .01 V^{-1}$

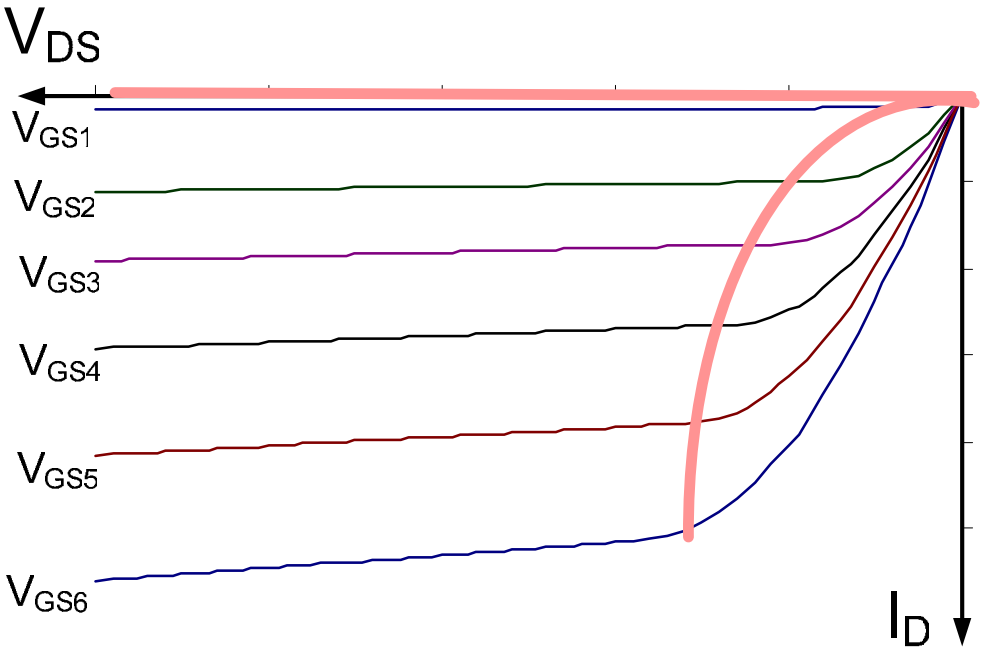
$V_T \approx 0.5V$ to $3V$

W/L varies by design

MOS Transistors



p-channel MOSFET



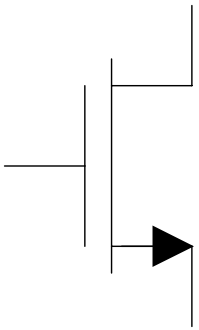
Standard square-law model

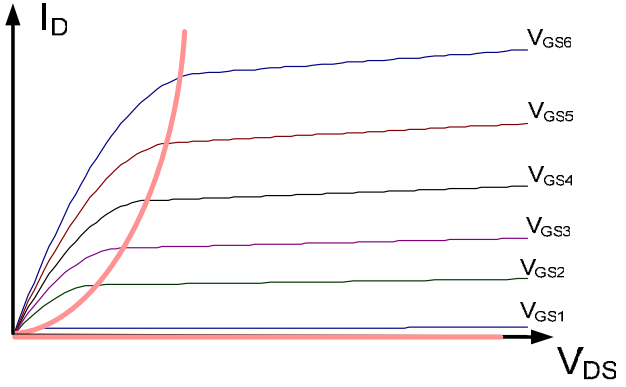
$I_G = 0$

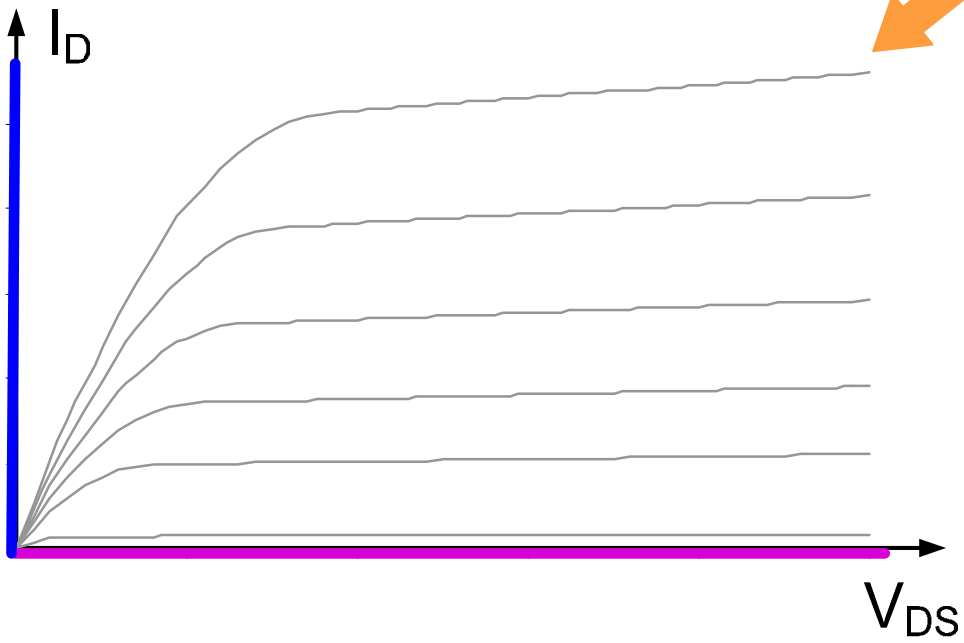
$$I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ \left(\frac{\mu C_{OX} W}{L}\right)\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \le V_T \quad V_{DS} \ge V_{GS} - V_T \quad \text{Triode} \\ \left(\frac{\mu C_{OX} W}{2L}\right)(V_{GS} - V_T)^2(1+\lambda V_{DS}) & V_{GS} \le V_T \quad V_{DS} < V_{GS} - V_T \quad \text{Saturation} \end{cases}$$

$V_T < 0$
$I_D \le 0$
$V_{DS} \le 0$

MOS Transistor Models
simplifications







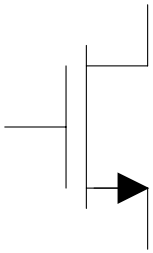
$I_G = 0$

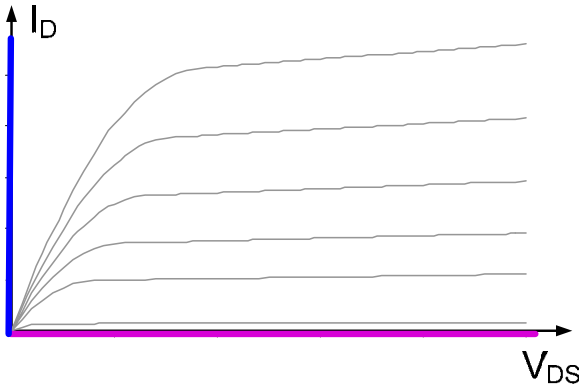
$I_D = 0$	$V_{GS} < V_T$	Cutoff
$V_{DS} = 0$	$V_{GS} \geq V_T$	Triode

Switch-level dc model – *good enough for predicting basic operation of many digital circuits*

MOS Transistor Models

simplifications



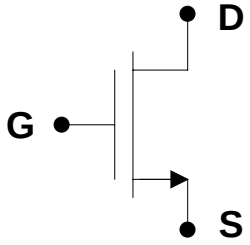


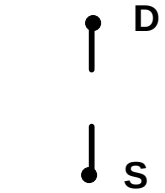
$I_G=0$

$I_D=0$ $V_{GS}<V_T$ Cutoff

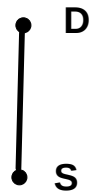
$V_{DS}=0$ $V_{GS} \geq V_T$ Triode

Equivalent Circuit Models

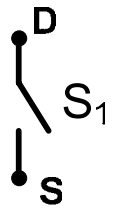




$V_{GS}<V_T$



$V_{GS}>V_T$

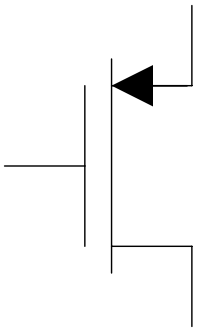


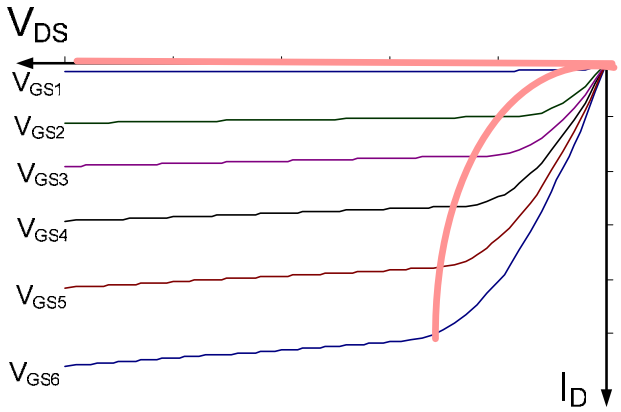
S_1 open for $V_{GS}<V_T$

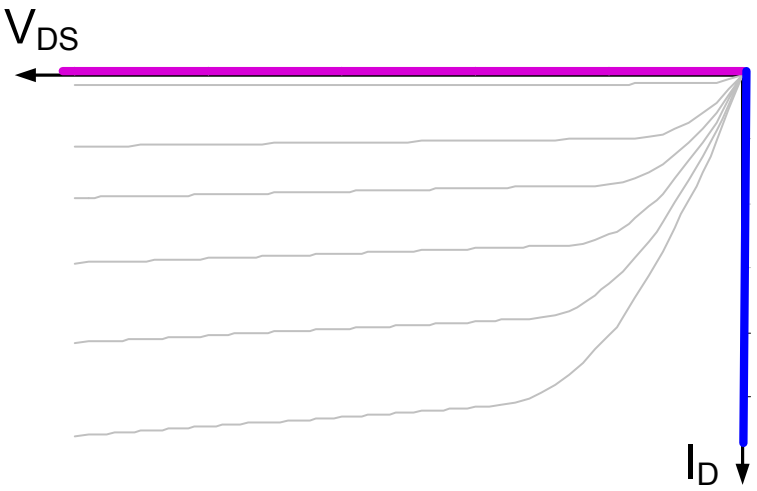
S_1 closed for $V_{GS}>V_T$

MOS Transistor Models

simplifications







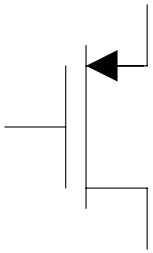
$I_G = 0$

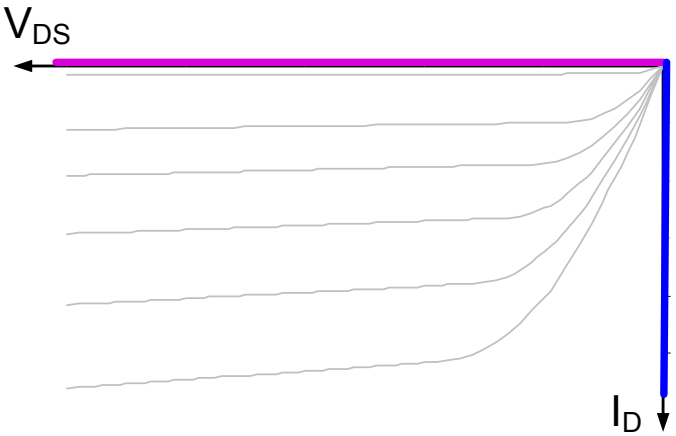
$I_D = 0$	$V_{GS} > V_T$	Cutoff
$V_{DS} = 0$	$V_{GS} \leq V_T$	Triode

Switch-level dc model – *good enough for predicting basic operation of many digital circuits*

MOS Transistor Models

simplifications



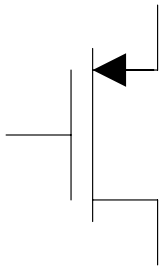


$I_G = 0$

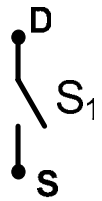
$I_D = 0$ $\quad V_{GS} > V_T$ $\quad$ Cutoff

$V_{DS} = 0$ $\quad V_{GS} \leq V_T$ $\quad$ Triode

Equivalent Circuit Models



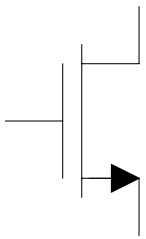
$V_{GS} > V_T$ $\quad V_{GS} < V_T$

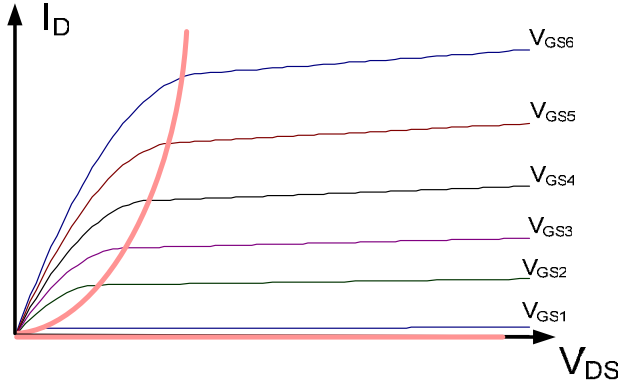


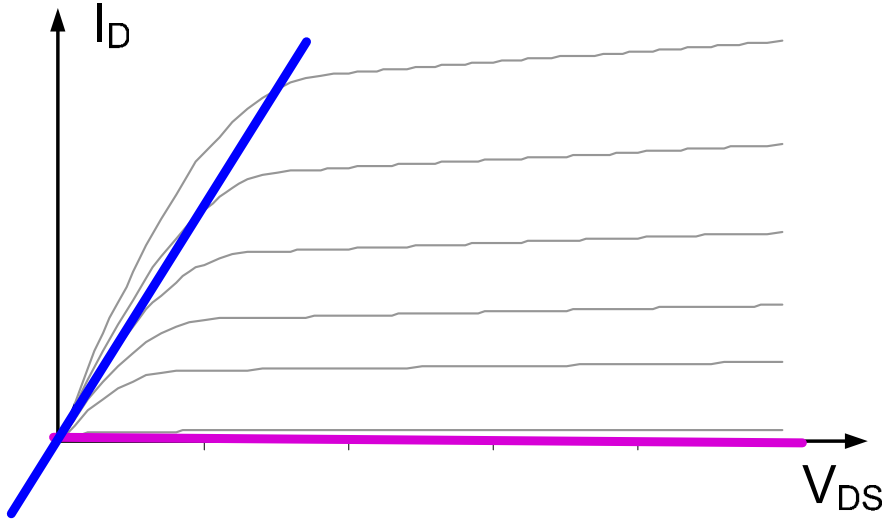
S_1 open for $V_{GS} > V_T$

S_1 closed for $V_{GS} < V_T$

MOS Transistor Models
simplifications







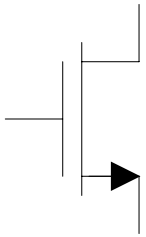
$$I_G = 0$$

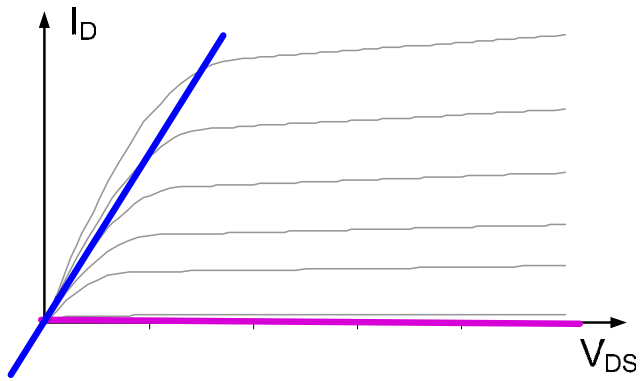
$$I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ V_{DS} / R_{FET} & V_{GS} \geq V_T \quad \text{Triode} \end{cases}$$

$$R_{FET} \cong \frac{1}{V_{GS} - V_T} \left(\frac{L}{\mu C_{OX} W} \right)$$

Better Switch-level dc model – *good enough for predicting basic operation of many digital circuits and can be used to predict speed performance if parasitic capacitances are added*

MOS Transistor Models
simplifications





$I_G = 0$

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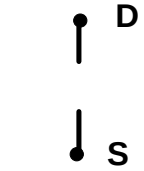
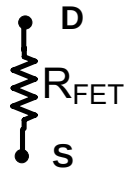
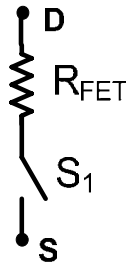


$V_{GS} < V_T$



$V_{GS} > V_T$

$$R_{FET} \cong \frac{1}{V_{GS} - V_T} \left(\frac{L}{\mu C_{OX} W} \right)$$

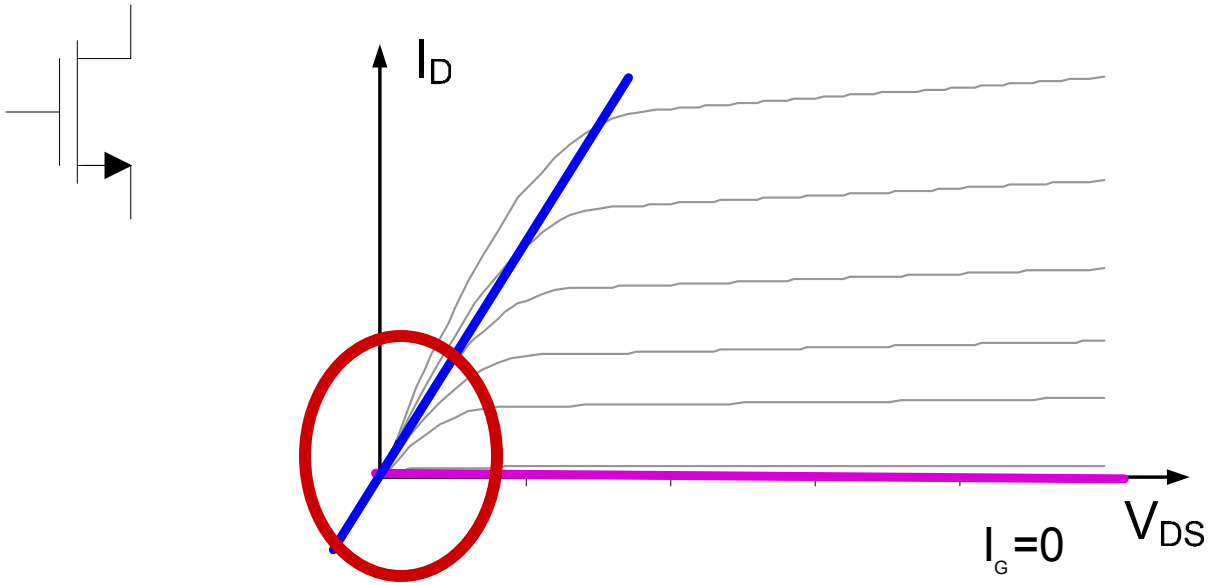


S_1 closed for $V_{GS} > V_T$

S_1 open $V_{GS} < V_T$

MOS Transistor Models

Voltage Variable Resistor (VVR) operation



$$R_{FET} \cong \frac{1}{V_{GS}-V_T}\left(\frac{L}{\mu C_{OX} W}\right)$$

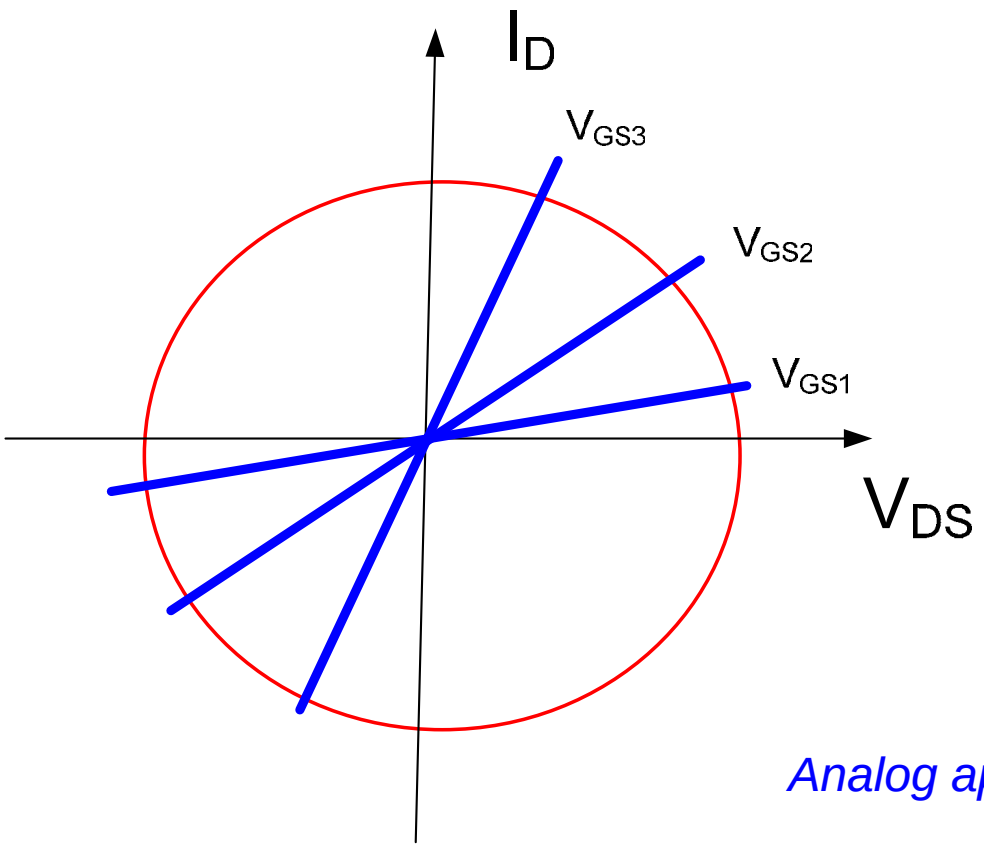
$$I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ V_{DS}/R_{FET} & V_{GS} \geq V_T \quad \text{Triode} \end{cases}$$

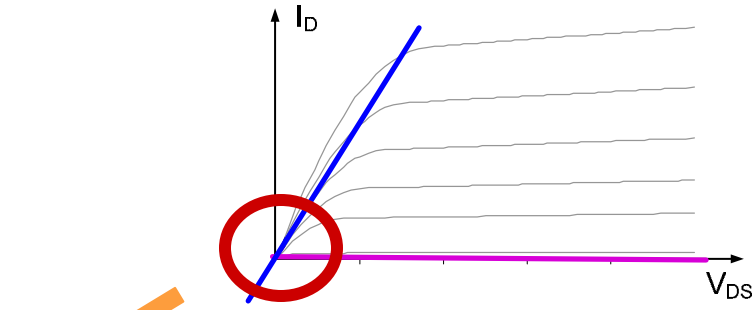
VVR Application – *dc gate to source voltage can be used to control the resistance*

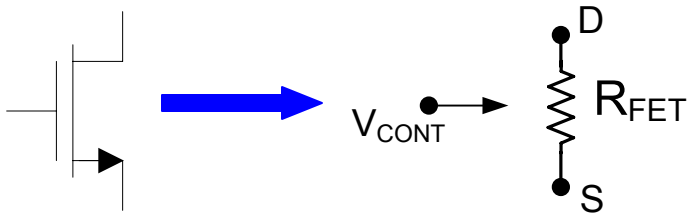
Widespread applications in analog circuits and computer-control of electronic circuits

MOS Transistor Models

Voltage Variable Resistor (VVR) operation



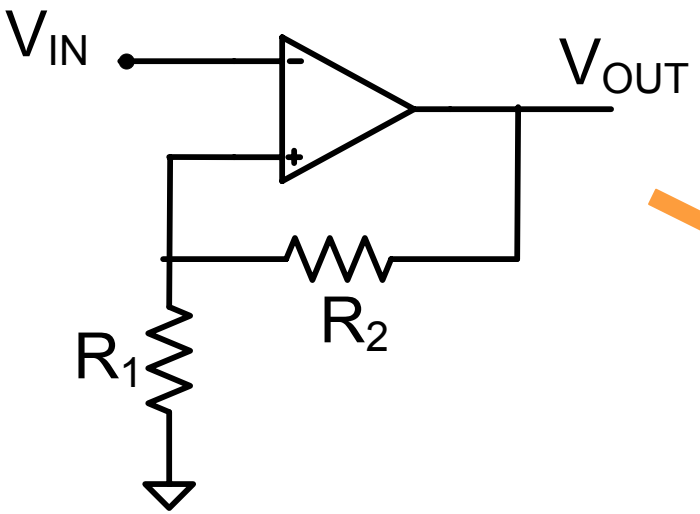


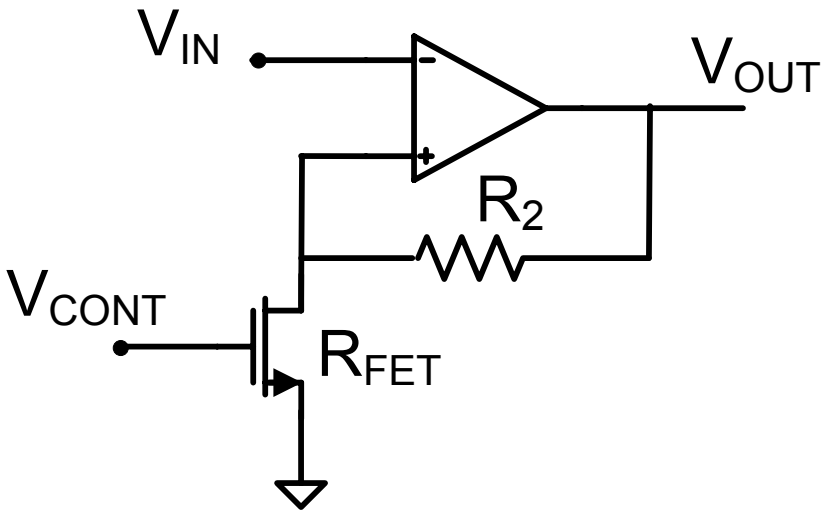


$$R_{FET} \cong \frac{1}{V_{GS}-V_T}\left(\frac{L}{\mu C_{OX} W}\right)$$

Analog application of MOSFET in triode region

Voltage Variable Resistor





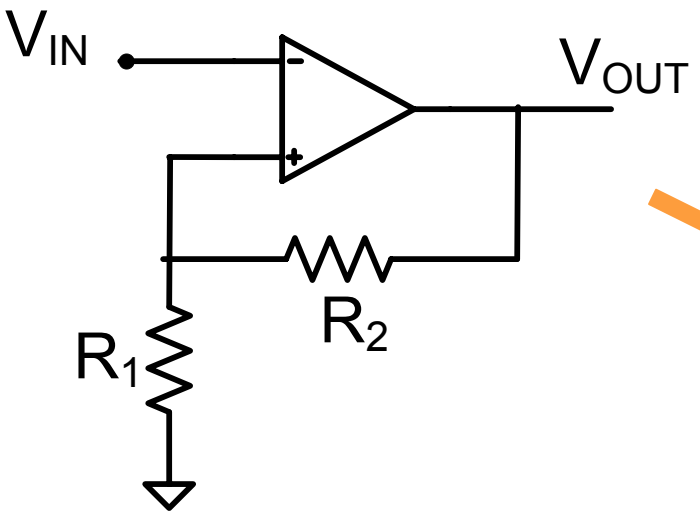
$$A_V = 1 + \frac{R_2}{R_1}$$

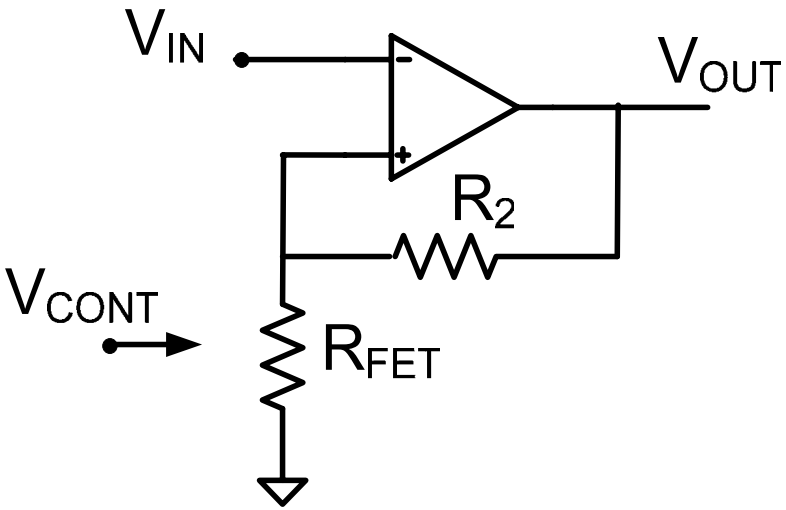
$$A_V = 1 + \frac{R_2}{R_{FET}}$$

$$R_{FET} \cong \frac{1}{V_{GS} - V_T} \left(\frac{L}{\mu C_{OX} W} \right)$$

Applications include Automatic Gain Control (AGC)

Voltage Variable Resistor





$$A_V = 1 + \frac{R_2}{R_1}$$

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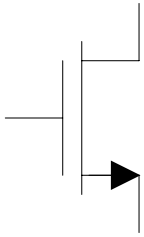
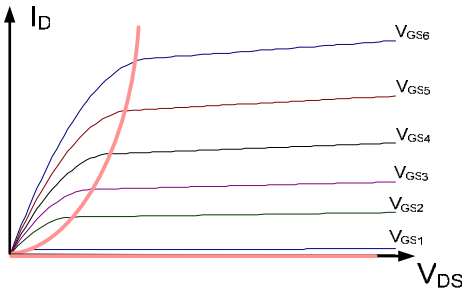
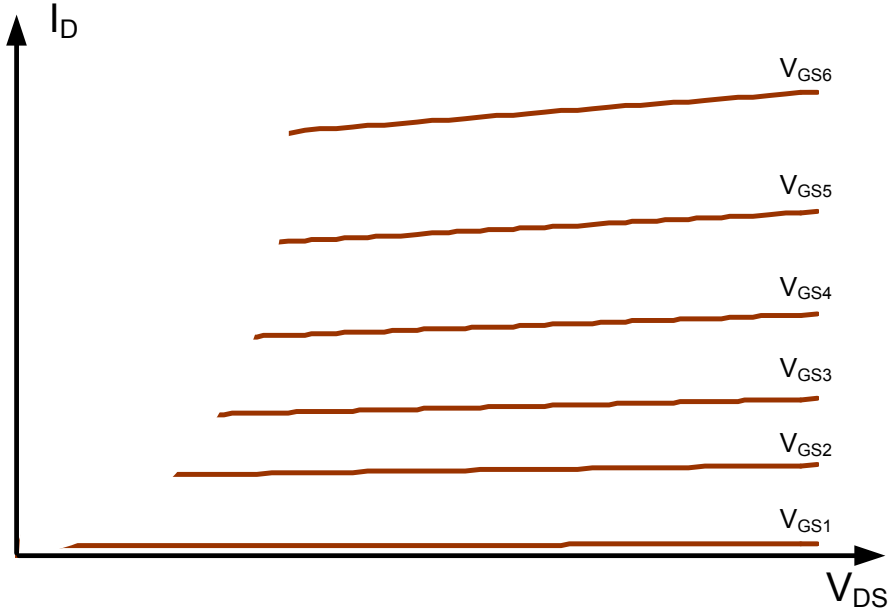
Applications include Automatic Gain Control (AGC)

MOS Transistor Models
simplifications







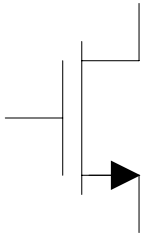
$$I_G = 0$$

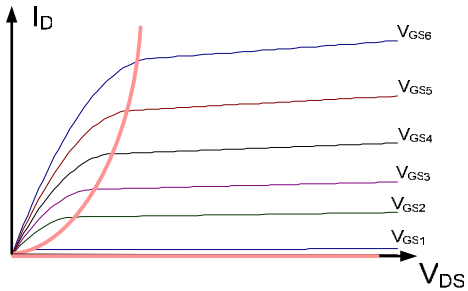
$$I_D = \left(\frac{\mu C_{OX} W}{2L}\right)(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \textbf{\textit{Saturation}}$$

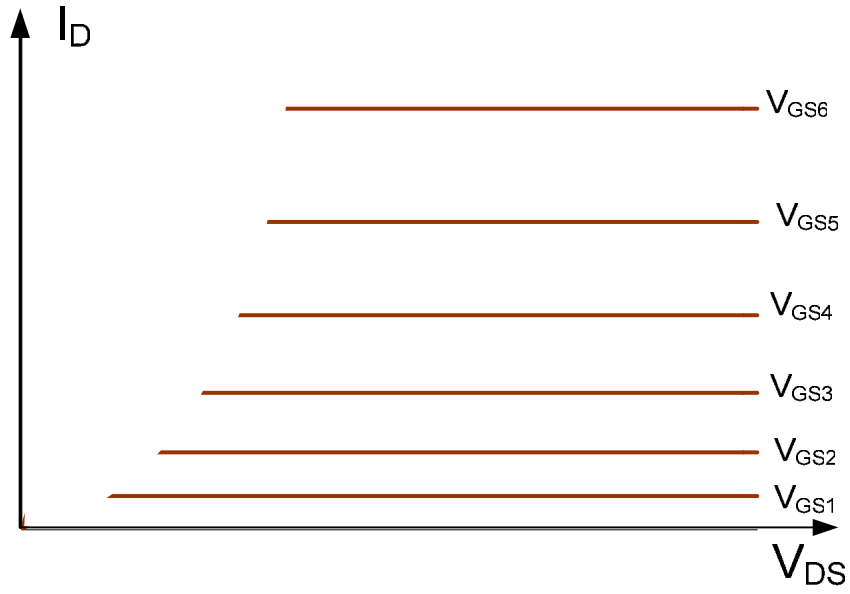
Can often assume $\lambda = 0$

Saturation Region Model – *used for many analog applications*

MOS Transistor Models
simplifications







$$I_G = 0$$

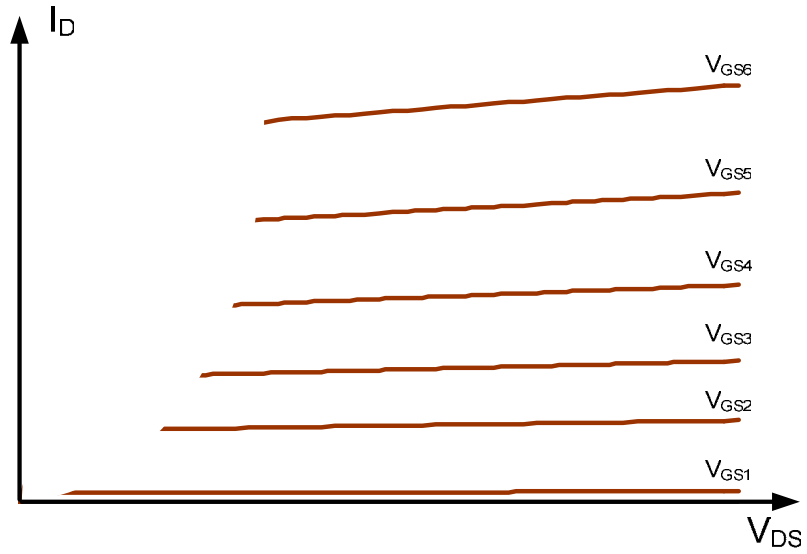
$$I_D = \left(\frac{\mu C_{OX} W}{2L}\right)(V_{GS} - V_T)^2$$

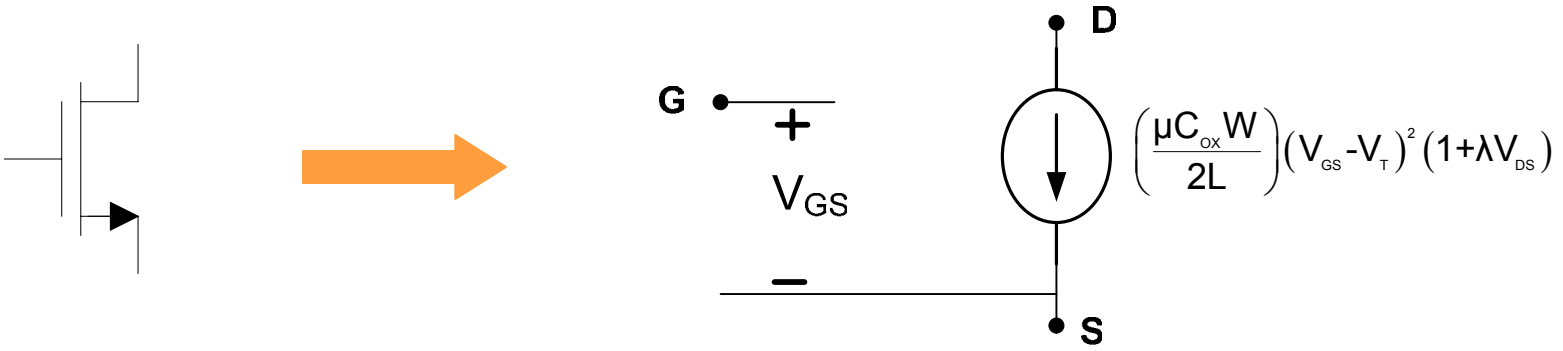
Saturation

With λ=0

Saturation Region Model – *good enough for many analog applications*

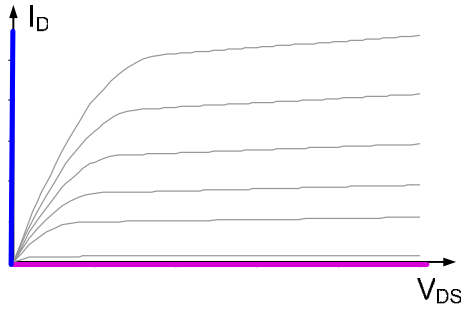
MOS Transistor Models
simplifications

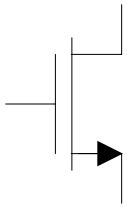


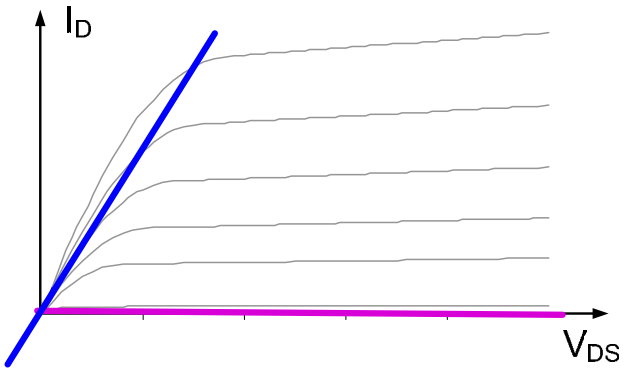


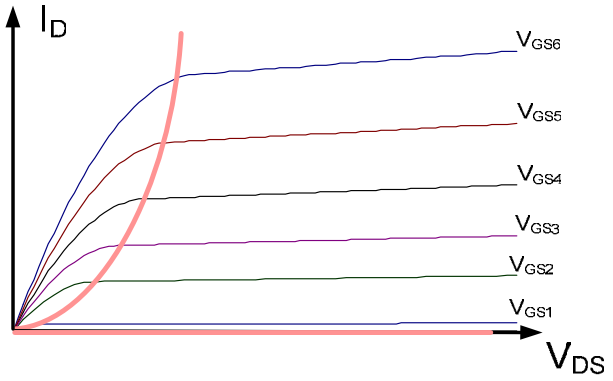
Saturation Region Model – *good enough for many analog applications*

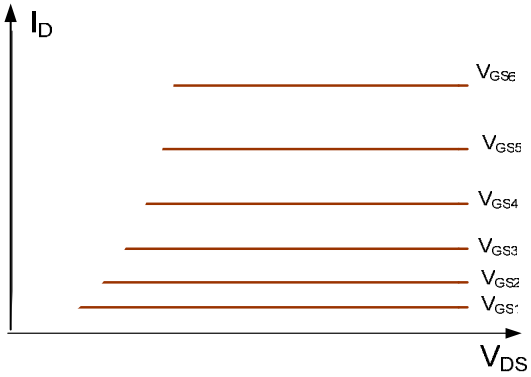
MOS Transistor Models (Summary)

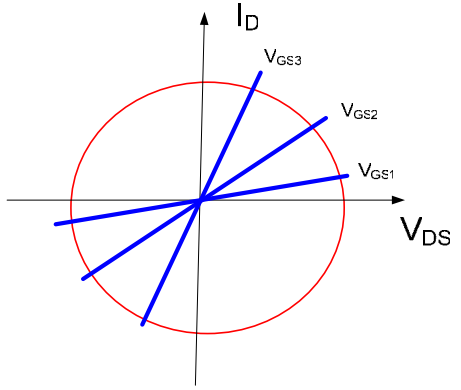




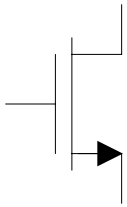


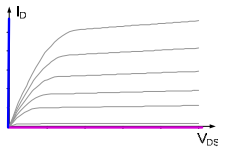


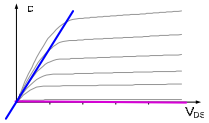


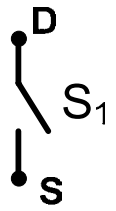


MOS Transistor Models (Summary)



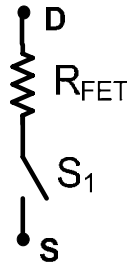






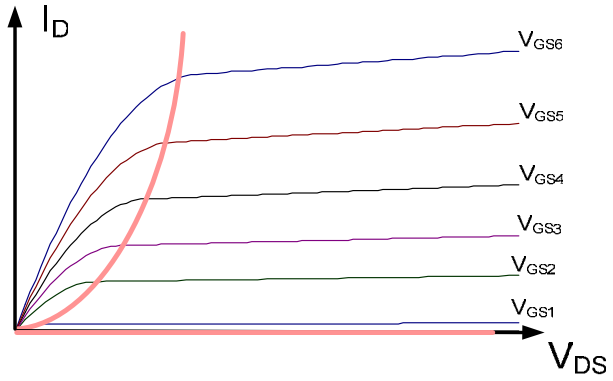
S_1 open for $V_{GS}<V_T$

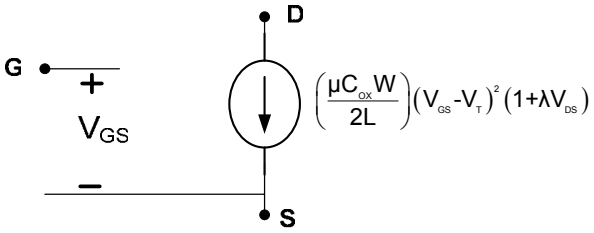
S_1 closed for $V_{GS}>V_T$

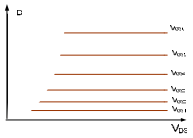


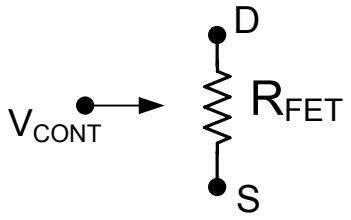
S_1 closed for $V_{GS}>V_T$

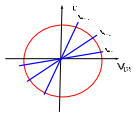
S_1 open $V_{GS}<V_T$



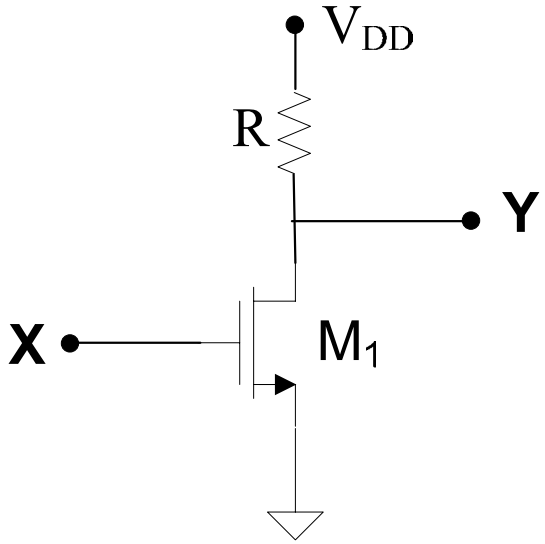








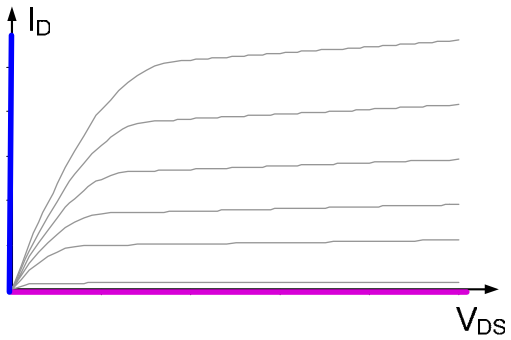
MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

MOSFET Model

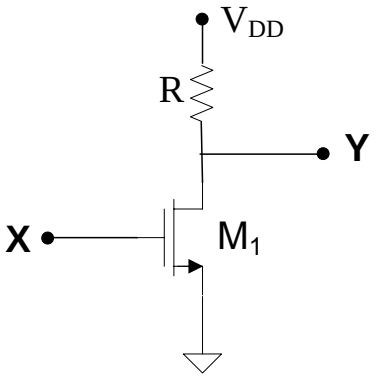


$I_G = 0$

$I_D = 0$	$V_{GS} < V_T$	Cutoff
$V_{DS} = 0$	$V_{GS} \geq V_T$	Triode

Assume $V_T \sim V_{DD}/5$

MOS Transistor Applications (Digital Circuits)



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Assume "0" ~ $V_L = 0V < V_T$

$I_D=0$ $V_{GS}<V_T$ Cutoff

$V_{DS}=0$ $V_{GS} \geq V_T$ Triode

Assume $V_T \sim V_{DD}/5$

If "1"~ **X**= V_{DD}, V_{DS}= 0V so Y = 0V ~ *"0"*

If "0"~ **X**= 0V, I_D= 0A so Y =V_{DD}-I_DR = V_{DD} ~ "1"

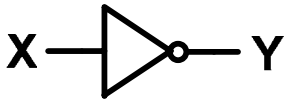
So this circuit performs as a Boolean inverter

Assume "0" ~ $V_L < V_T$

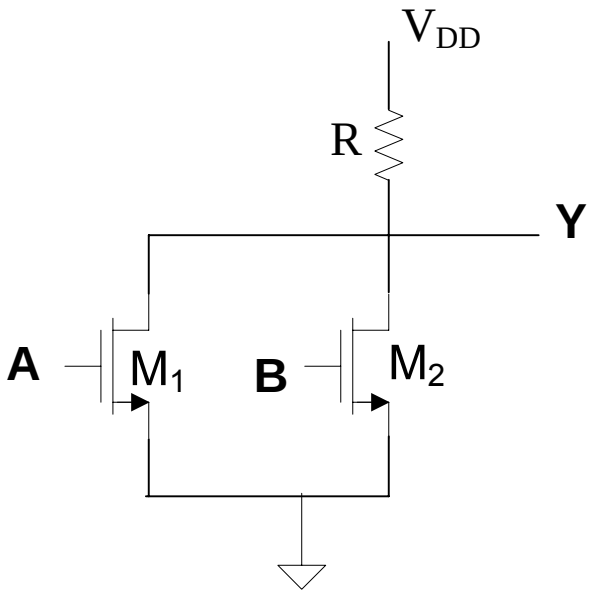
Assume "1" ~ $V_H > V_T$

X	Y
0	1
1	0

Truth Table



MOS Transistor Applications (Digital Circuits)



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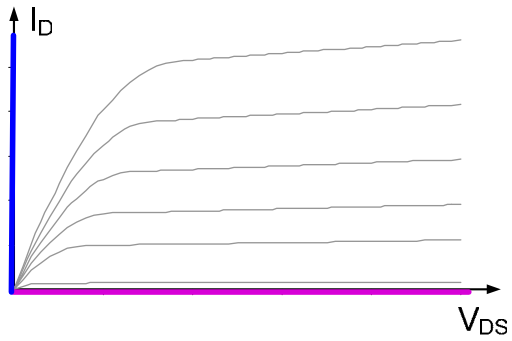
MOSFET Model



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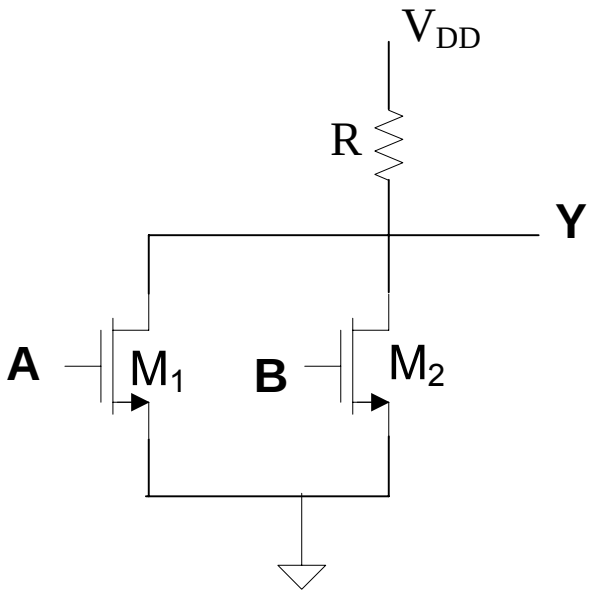
MOS Transistor Applications (Digital Circuits)



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$V_{DS} = 0$ $V_{GS} \geq V_T$ Triode

Assume $V_T \sim V_{DD}/5$

If "1"~ **A**= V_{DD}, "1"~ B= V_{DD}, $V_{DS1}=V_{DS2}= 0V$ so Y = 0V ~ *"0"*

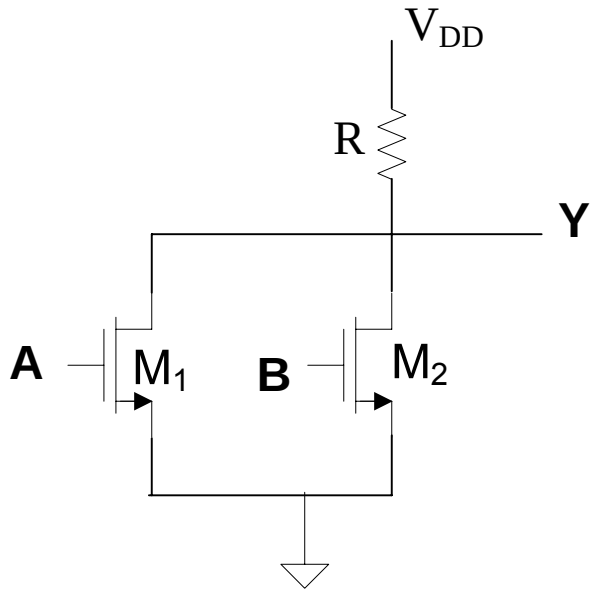
If "1"~ **A**= V_{DD}, "0"~ B= 0V, $V_{DS1}= 0V$ *(and $I_{D2}=0A$)* so Y = 0V ~ *"0"*

If "0"~ **A**= 0V, "1"~ B= V_{DD}, $V_{DS2}= 0V$ *(and $I_{D1}=0A$)* so Y = 0V ~ *"0"*

If "0"~ **A**= 0V, "0"~ B= 0V, $I_{D2}= 0A$ *and $I_{D1}=0A$* so $I_R=0A$, thus

Y = $V_{DD} = I_R R = V_{DD}$ ~ *"1"*

MOS Transistor Applications (Digital Circuits)



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

If "1"~ **A**= V_{DD}, "1"~ B= $V_{DD,}$ V_{DS1}=V_{DS2}= 0V so Y = 0V ~ *"0"*

If "1"~ **A**= V_{DD}, "0"~ B= 0V, V_{DS1}= 0V *(and* I_{D2}*=0A)* so Y = 0V ~ *"0"*

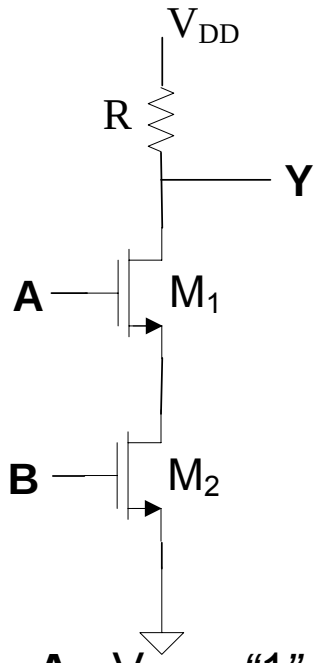
If "0"~ **A**= 0V, "1"~ B= $V_{DD,}$ V_{DS2}= 0V *(and* I_{D1}*=0A)* so Y = 0V ~ *"0"*

If "0"~ **A**= 0V, "0"~ B= 0V, I_{D2}= 0A *and* I_{D1}*=0A* so I_R=0A, thus

Y = V_{DD}= I_RR=V_{DD} ~ *"1"*

2-input NOR Gate

MOS Transistor Applications (Digital Circuits)



Assume "1" ~ $V_H = V_{DD} > V_T$

Assume "0" ~ $V_L = 0V < V_T$

$I_D = 0$ $V_{GS} < V_T$ Cutoff

$V_{DS} = 0$ $V_{GS} \geq V_T$ Triode

Assume $V_T \sim V_{DD}/5$

If "1"~ **A**= V_{DD}, "1"~ B= V_{DD}, $V_{DS1}=V_{DS2}= 0V$ so Y =0V ~ *"0"*

If "1"~ **A**= V_{DD}, "0"~ B= 0V, $V_{DS1}= 0V$ and $I_{D2}=0A$ so $I_R=0A$ thus

$Y = V_{DD} - I_R R = V_{DD}$ ~ "1"

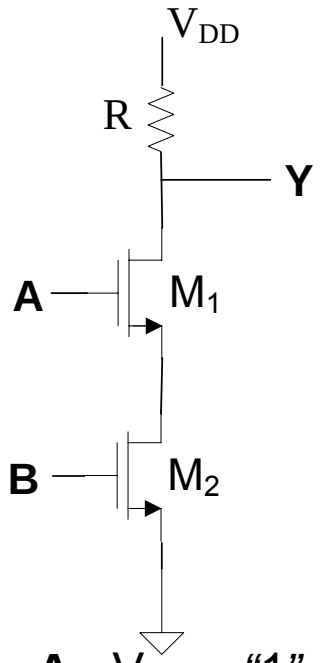
If "0"~ **A**= 0V, "1"~ B= V_{DD}, $V_{DS2}= 0V$ and $I_{D1}=0A$ so $I_R=0A$ thus

$Y = V_{DD} - I_R R = V_{DD}$ ~ "1"

If "0"~ **A**= 0V, "0"~ B= 0V, $I_{D1}= 0A$ and $I_{D2}=0A$ so $I_R=0A$ thus

$Y = V_{DD} - I_R R = V_{DD}$ ~ "1"

MOS Transistor Applications (Digital Circuits)



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

If "1"~ **A**= V_{DD}, "1"~ B= V_{DD}, V_{DS1}=V_{DS2}= 0V so Y =0V ~ *"0"*

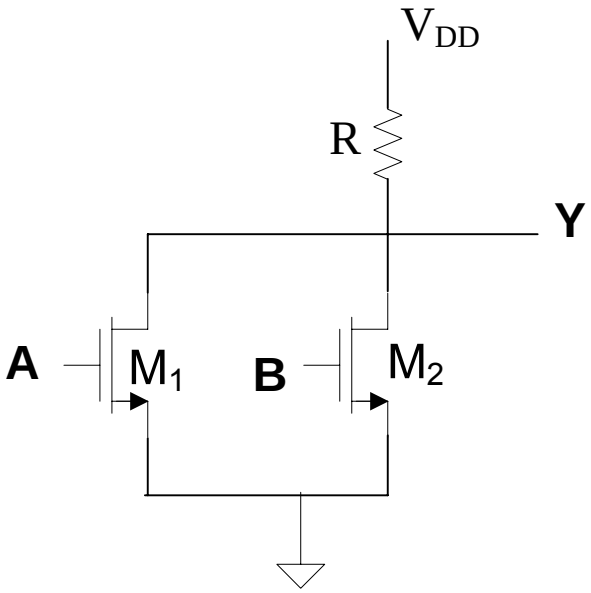
If "1"~ **A**= V_{DD}, "0"~ B= 0V, V_{DS1}= 0V and I_{D2}=0A so I_R=0A thus
Y =V_{DD}-I_RR= V_{DD} ~ "1"

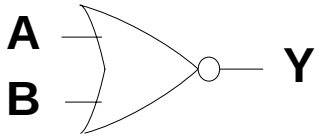
If "0"~ **A**= 0V, "1"~ B= V_{DD}, V_{DS2}= 0V and I_{D1}=0A so I_R=0A thus
Y =V_{DD}-I_RR= V_{DD} ~ "1"

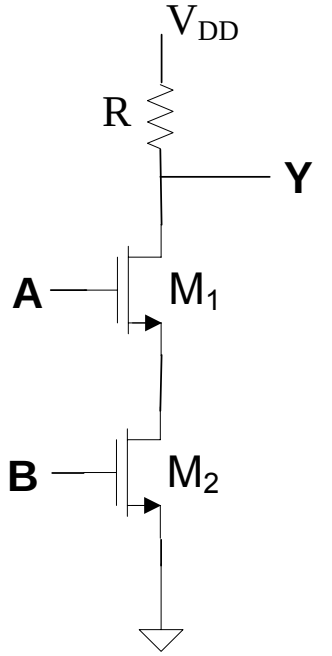
If "0"~ **A**= 0V, "0"~ B= 0V, I_{D1}= 0A and I_{D2}=0A so I_R=0A thus
Y =V_{DD}-I_RR= V_{DD} ~ "1"

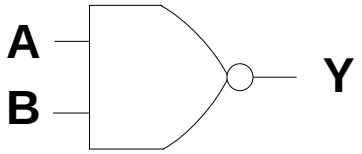
2-input NAND Gate

MOS Transistor Applications (Digital Circuits)









- Can be extended to arbitrary number of inputs
- But the resistor is not practically available in most processes and static power dissipation is too high